Abstract of the Disclosure

A non-volatile memory device includes a cell region having a memory gate pattern with a charge storage layer, and a peripheral region having a high-voltage-type gate pattern, a low-voltage-type gate pattern, and a resistor pattern. To fabricate the above memory device, a device isolation layer is formed in a substrate. Gate insulating layers having difference thickness are formed in low-and high-voltage regions of the peripheral region, respectively. A first conductive layer is formed over substantially the entire surface of a gate insulating layer in the peripheral region. A triple layer including a tunneling insulating layer, a charge storage layer, and a blocking insulating layer and a second conductive layer are sequentially formed over substantially the entire surface of the substrate including the first conductive layer.